MULTIPLE VOLTAGE SEQUENCING WITH THE MPGS-14A

Hi-Rel Grade

Sequencing and synchronizing several Points of Load

AN5005056

- 1.2 to 24V out step-down converter
- FPGA, µC multiple supply
- Coincident -rationmetric -offset sequencing
- Trimmable start up 3ms to 30ms
- Nominal current up to 14 A

1-Foreall

The question of synchronizing the start-up sequence of each channel arise as soon as a designer needs to supply several subcircuits of a given application with various voltages levels.

Common examples are FPGA and CPU based designs that require multiple low voltages to supply cores and I/O stages.

The challenge for the designer is to apply the different voltages with the correct sequence and timings to meet each IC specific requirement.

GAIA CONVERTER MPGS14EB is a highly configurable **Military grade Point of Load** that features all necessary functions to achieve the most complex start-up sequences in a simple way.

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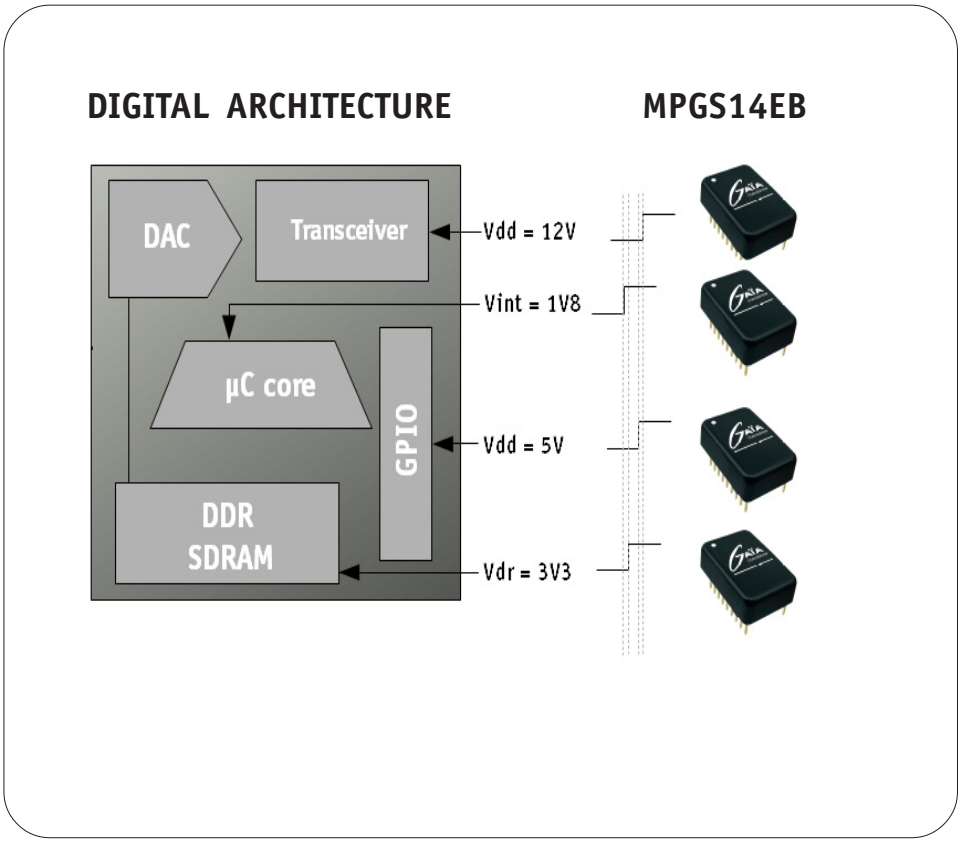
2-Multiple Voltage sequencing



3- Offset sequencing

The offset sequencing scheme allows to introduce a delay between each voltage rail start-up.
In the example presented in figure 1, three MPGS14EB are implemeted to deliver a 12V, a 5V and a 3.3V.
The resistor connected to Vtrim of MPGS14EB is used to program the output voltage of the given channel. With no resistor the output voltage is by default 3.3V.
A resistor across Vtrim and GND will trim up the output voltage above 3.3V. A resistor between Vtrim and Vout will trim down the output voltage between 1.2 and 3.3V.

An external capacitor connected to the UVLO pin is used to delay the start-up of each MPGS14EBs.

By using different capacitor values on each UVLO pin, it is possible to shift the start-up of each MPGS14EB and to control the order in which each output voltage is applied. The time-shift can be evaluated with the following equation :

$$t_d(ms) = 0{,}013 \cdot [10 + C_{ext}(nF)] \cdot \ln\left(\frac{Vin}{Vin - 4{,}5}\right)$$

Where :
td = start-up time in ms.
Cext = capacitor connected to SD_UVLO in nF.
Vin = Input voltage in Volt.

Such a configuration delaying the turn-on time with a capacitor connected accros the Shutt-down pin can be used to power-up different blocks at defined times. Figure 2 shows the output voltages for each channel.

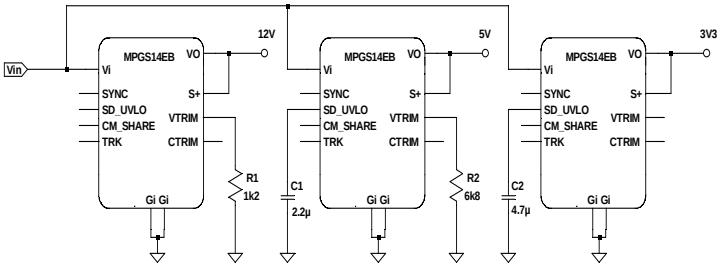


Figure-1: 3 rails Offset sequencing

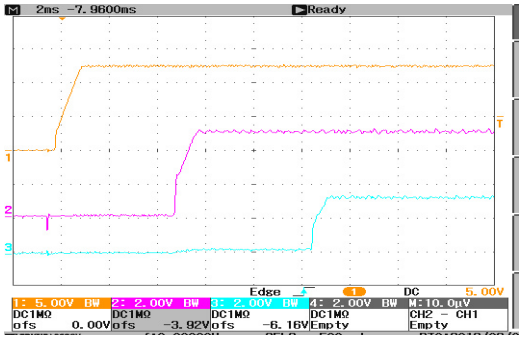
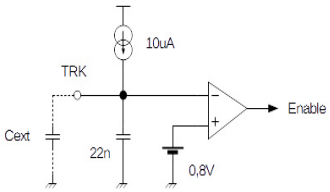


Figure-2: 3 rails Output voltage

4- Ratiometric sequencing

A different way to achieve a time-shifted sequence is to implement the tracking function as per schematic on figure 3. The tracking function of MPGS14EB allows to control the start-up ramp of the output voltage by charging an external capacitor to 0,8V with an internal 10uA current generator as shown on the internal schematic diagram below.



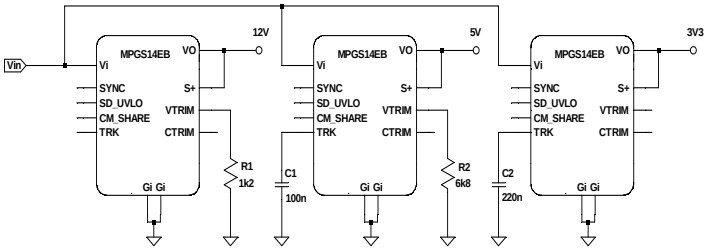


Figure-3: 3 channels with delayed outputs

4- Ratiometric sequencing (continued)

The start-up time can then be calculated from the equation :

$$t_{start}(ms) = 0{,}08 \cdot [C(nF) + 22]$$

Where :
t_{start} = is the start-up time in ms.
C= capacitor connected to Tracking function pin (trk).

Here again, by using different capacitors, it is possible to generate different slopes, so that each output voltage reaches its final value at a determined time, as illustrated on the figure 4. Note that compared with the previous situation, here all outputs start-up simultaneously whereas they reach their final value depending on the capacitor set implemented.

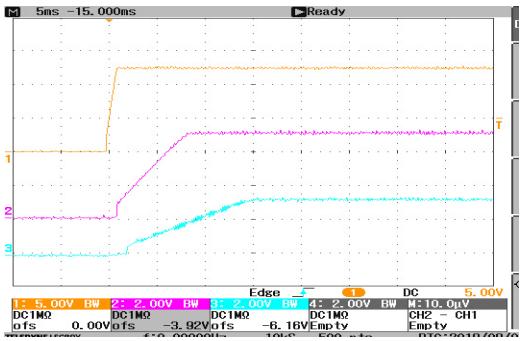


Figure-4: Multiple voltages slopes

Ratiometric:

If the same capacitor is used on each unit (or if all MPGS14 are used with no capacitor on TRK), all outputs will power-up simultaneously and also reach their final value at the same time. This start-up mode is known as ratiometric start-up.
This mode of operation is specially usefull for application where it is essential to start operation for each device at the exactly same time.
The graph on the figure 6 shows the rise of 3 channels with 100nF on each TRK pin.

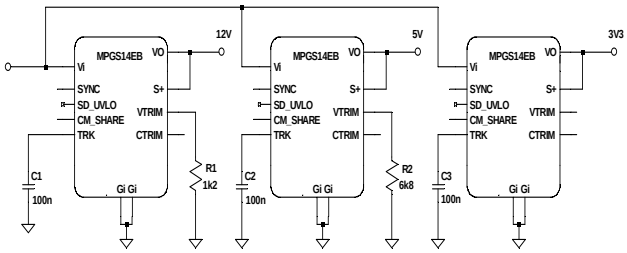


Figure-5: Ratiometric sequencing

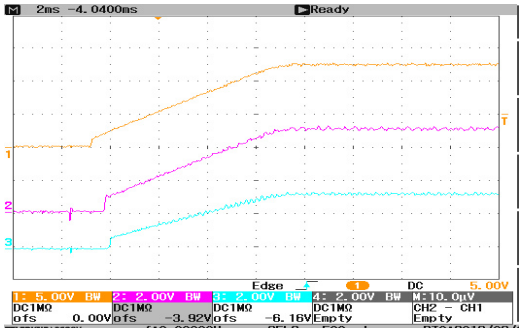


Figure-6: Ratiometric sequencing

5- Coïncident sequencing

The last start-up sequence allowed by MPGS14EB is known as coïncident tracking. In this mode, the PoL with the highest voltage acts as a master and drives the start-up of the other voltages. This is achieved by using an external resistor bridge to drive the TRK pin as per schematic figure 5 .

Each resistor bridge is calculated so that the voltage at the TRK pin is 0,8V when the driving voltage, here the 12V, is equal to the nominal output voltage of the driven PoL.

As an example, when the 12V output reaches 5V, the voltage generated at the TRK pin by R1 and R2 bridge is 5V and the 5V PoL is then enabled. In this way, the 12V and the 5V « coïncides » with each other. Figure 7 shows the resulting start-up sequence when such a mode is implemented.

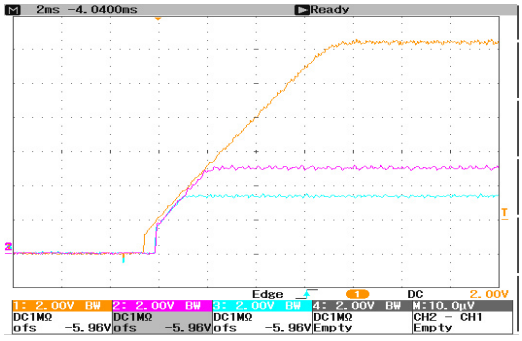


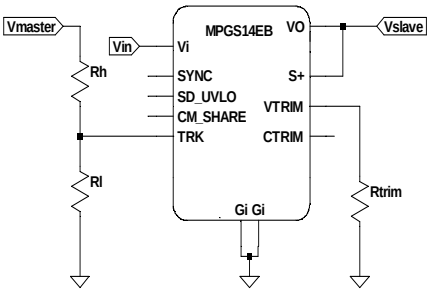
Figure-7: Ratiometric sequencing

5- Coïncident sequencing (continued)

As can be seen, when the 12V reaches 3.3V, it enables the 3.3V PoL, and when it crosses 5V, the 5V PoL is enabled in turn. In this mode, it should be noted that the lower output voltages are enabled in priority. The formula to determine the resistor bridges as a function of the « coincidence » voltage is

$$R_h = \left(\frac{Vo_{slave}}{0.8} - 1\right) \cdot R_l$$

Wherer :
Rh = top side resistance of the bridge.
Voslave = nominal output voltage of driven MPGS14.
Rl = low side resistance of the bridge.



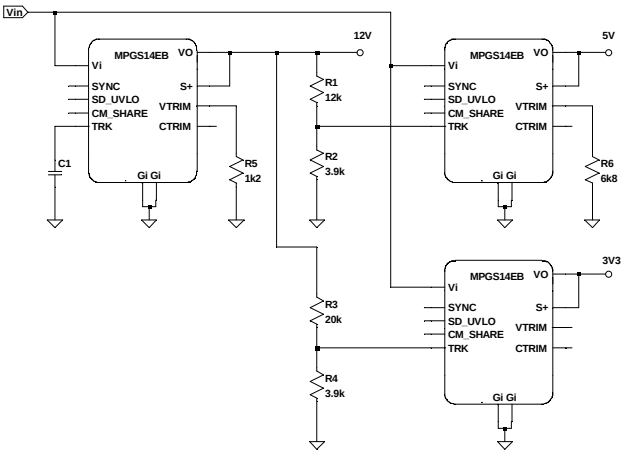


Figure-8: Coincident sequencing

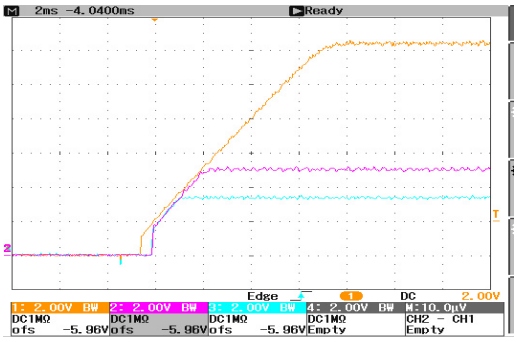


Figure-9: Coincident sequencing

POSSIBLE RESISTOR VALUES FOR COINCIDENT SEQUENCING								
Slave Output Voltage	1.2 Vdc	2.7 Vdc	3.3 Vdc	5 Vdc	9 Vdc	12 Vdc	15 Vdc	24 Vdc
Rh (Kilo Ohm)	2.2	2.26	3.9	4.2	4.1	5.1	5.1	3.3
Rl (Kilo Ohm)	1.1	5.37	12.19	22.05	42.03	71.4	90.53	95.7

Resistor can be choosen in E96 serie

6- Conclusion

The MPGS14EB is a highly versatile Military grade Point of Load that can be configured to implement all types of start-up sequences with minimal external components. Its ease of use will greatly simplify voltages start-up management in digital designs. Other available features such as Synchronization, UVLO trim-up current monitor, and more make it one of the most complete and smartest PoL available today on the market.